Apollo 1 Chipset

Features

- Compliant with ANSI T1.413 Issue 2, ITU-T G.992.1 (G.dmt), and G.992.2 (G.lite)
- 2 chip transceiver including ATM framer
- Discrete multitone (DMT) modulation
- Full rate adaptive modem at 32 kbps steps
- Built-in ATM transport convergency layer
- FDM duplex
- Up to 8 Mbps downstream data rate
- Up to 640 kbps upstream rate
- Trellis coding capability
- Switchable ATU-R and ATU-C modes
- Reed-Solomon forward error correction
- Support of interleaved and fast paths
- Full and reduced ATM overhead options
- Low power 3V technology
- Direct connection to ATM systems (UTOPIA 1 and 2 interfaces)
- Bitstream mode capable for STM applications

Applications

- CO & CPE ADSL equipment
- DSL Access Multiplexers (DSLAM)
- ADSL PC NICs
- ADSL access for routers
- DLC upgrade
- ADSL line cards for ATM switches and multiplexers

General Description

The Apollo 1 is an ADSL modem solution consisting of an integrated Analog Front End (I80134) and a DMT transceiver and ATM framer (I90135). A dedicated controller with associated firmware, such as i960, is also required. The Apollo 1 provides all the active functions required to implement a complete ATM-based, rate adaptive DMT ADSL modem. As shown in figure 1, the chipset interfaces have been defined to allow direct integration into systems design, reducing both time-to-market and implementation risks.

The data interface is implemented as an ATM Utopia interface (non ATM mode also available). A HW/FW command and control interface (CTRLE), to communicate with external management entities, is required.

The chipset employs DMT modulation as specified in ANSI T1.413. Additional Reed-Solomon forward error correction with or without interleaving provides maximum noise immunity. The chipset can operate at either end of the loop (in ATU-C and ATU-R modes) with only changes in the controller code.

The ITeX ADSL Modem Chipset

Apollo 1 is a two-chip ADSL modem transceiver. The chipset directly interfaces with ATM traffic to allow ATM traffic to be transported at high speed on copper pairs with minimum overhead.

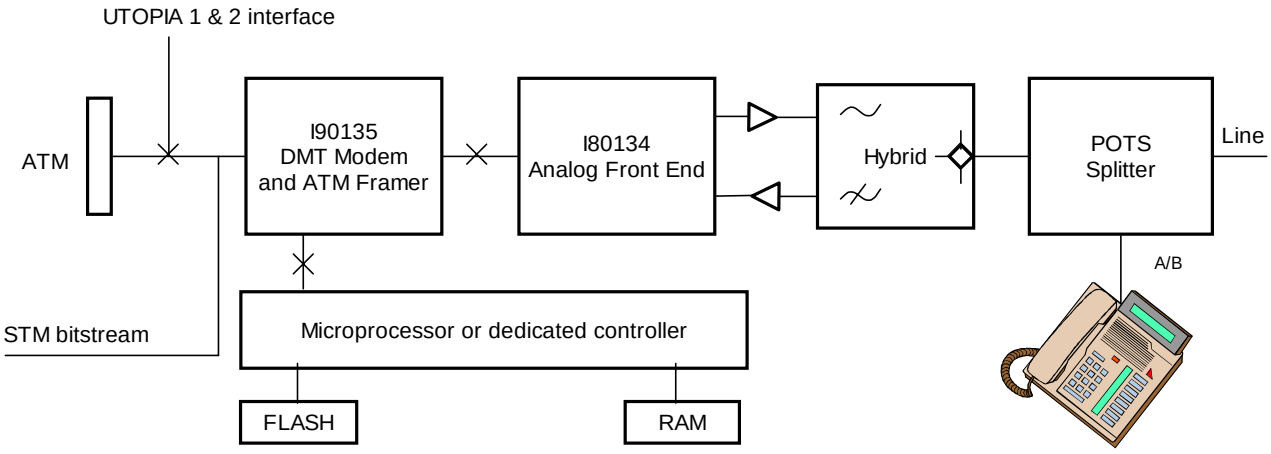

Figure 1.1: General Block Diagram

The Modem Environment

Although the required capabilities of the transceiver at the network termination and the local exchange points are not the same (ADSL is an asymmetrical transmission mode), the same chipset is used at both sides of the link. The ICs used to make the transceiver are controlled by one dedicated controller. An external ADSL-compatible line driver is used to drive the telephone twisted pair. Finally, an analog POTS splitter is needed to split the baseband analog telephone signal from the modulated ADSL signal. Brief characteristics of the system are given in Table 1. Table 2 shows speed versus distance in upstream and downstream directions. The bitrate can be varied in steps of 32 kbps.

The Chipset Functions

The chip functions are depicted in the block diagram of the ADSL modem presented in Figure 2.

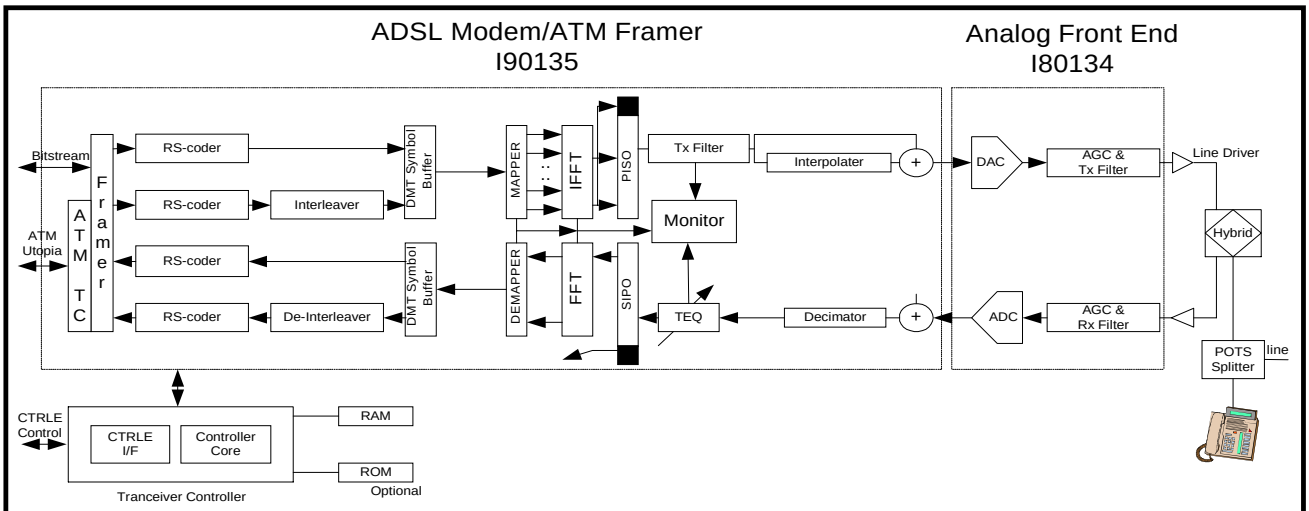

Fig. 2: ADSL Chipset Block Diagram

The functions included in each IC are as follows:

- **An Analog Front-end Circuit (I80134)**

This CMOS IC contains the analog functions required in the transceiver. In order to cope with the high attenuation of the line and in order to keep acceptable noise level of the signal, automatic gain control amplifiers have been implemented at the analog front of the transmission and reception paths. Then, the signal is passed through low pass filters to eliminate the echo signal and out-of-band interferences.

Depending on the configuration, ATU-C or ATU-R, upstream and downstream channel filter may be exchanged between the transmission and the reception channel.

The AD and DA converters provide 12 bit resolution at 8.8 MHz sampling rate. Finally, for the transmission part, the control of the external hybrid drivers is done by an integrated highly linear line pre-driver.

- **Modem/Framer (I90135)**

This CMOS IC contains all the digital functional blocks required for the following functions.

1) DMT Modulation and Demodulation
The I90135 implements digitally the Quadrature-Amplitude Modulation (QAM) mapper/ demapper, which allows up to 14 bits coding per tone (a constellation of 16383 points).

The device implements the necessary Inverse- and Fast Fourier Transform (IFFT, FFT), the Time- and Frequency-Domain Equalizer (TEQ, FEQ) plus timing

units and voltage controlled crystal oscillator (VCXO).

These last blocks implement efficient synchronization algorithms to improve the efficiency of the recovery of data.

2) Framing Functions
The I90135 implements framing functions for the generic and ATM Transmission Convergence (TC) layers. The generic TC consists of data scrambling and Reed Solomon enter correction with and without interleaving.

The ATM TC includes cell level functions (such as cell delineation, insertion/ extraction of idle cells, payload scrambling, HEC check) and data frame generation.

Several framing variants are implemented (such as interleaved and non-interleaved modes, full and reduced overhead) to ensure compliance with ANSI T1.41 3 Issue 2 and compatibility with other Issue 1 chipsets. For non-ATM applications (e.g. Frame Relay, PPP, ...), a bitstream mode is available which bypasses the ATM Framer.

3) Interface to ATMF Standard UTOPIA Bus
The IC contains the ATM related functions to interface with the ATM UTOPIA bus and supports level 1 and 2 modes.

ADSL transceiver controller
A dedicated transceiver controller, such as i960 or similar microcontroller, is required for the control of the ADSL Transceiver. It runs the ADSL FW and communicates with external management entities through a specific modem command interface "control E" (CTRLE). The chip runs the FW controlling the operations of the I90135 and I80134. During modem initialization, the controller computes and sets up parameters or all programmable DINT functions, filters and equalizers. The controller is able to run in different rate-adaptive modes as defined by the operator and can run programs for the ATU-C (master mode) or for the ATU-R (slave mode) sides. During operation, the controller performs continuous line monitoring and initiates consecutive actions as specified by the operator (e.g. bit-swapping. dynamic bitrate adaptation,...) and collects performance and error information for use by management entities.

The controller also runs the communi-cation protocol to interface with external management entities. A specific ADSL modem control interface has been defined to ease the integration with both systems HW and FW. This so-called CTRLE communication channel is used to transfer information and commands between modem and management entities. These commands/responses can be categorized as follows:

- Configuration of a modem line
- De-allocation of a modem line
- Operational Data Retrieval
- Performance Data Retrieval
- Defect Retrieval

The controller provides direct HW connection to external components (processors, SARs. Muxes,...) through either 8-bit parallel or serial bus.

Table 1: Summary of Characteristics ADSL Chips

I80134
- 4.3 kHz tone spacing
- ADC 12 bit resolution, 8.832 MHz sampling rate
- DAC 12 bit resolution. 8.832 MHz sampling rate
- Analog/tunable low-pass filters
  - Upstream channel fc 138 kHz, <1dB ripple
  - Downstream channel fc 1100 kHz, <1 dB ripple
- AGC range: 0..31 dB in steps of 1 dB (Rx)
  -15..0 dB in steps of 1 dB (Tx predriver)
- Package: 64 LQFP

I90135
- DMT modulation
  - max. number of bit per tone: 14 bits (16383 constellation points)
  - max. number of tones: 256 tones
- Max. clock speed: 36 MHz
- Max. tone spacing: 4.325 kHz
- RS encoder: max codeword 256 bytes
- ATM Processor:
  - ATM cell buffering
  - Cell counting
  - Insert/Extract, Idle/Unassigned ATM cells (rate adaptation)
  - ATM HEC generation module (CCITT 1.432)
  - ATM payload scrambler: payload width: 48 bytes
- UTOPIA Level 2 Interface
- Bitstream interface
- Package: 144 PQFP

Table 2: Performance Simulations

Distances	**Data rate at 6dB margin**	
0.4 mm 26 AWG	**Upstream**	**Downstream**
0.9 km - 3 kft	800 kbps	8 Mbps
2.7 km - 9 kft	640 kbps	6 Mbps
3.6 km - 12 kft	640 kbps	4 Mbps
4.5 km - 15 kft	640 kbps	2 Mbps

Building Systems with Apollo1

Great care has been taken in defining the Apollo 1 to ease its integration into system designs. In particular, this is achieved:

- at HW level: by using standard interfaces data transfer (ATM Utopia)

and for control (8 bit parallel or serial bus)

- at FW level: by clearly separating the modem FW, run on the dedicated transceiver controller from other systems related and application specific functions. The boundary between the two domains is provided by means of a simple modem control protocol (CTRLE).

This "packaged modem" approach provides a self-contained ADSL modem solution, allowing system manufacturers to concentrate on system issues.

The Apollo 1 comes in a full package with Bill of Material and layout information for the ADSL modem part.