



I90135-ADSL Digital Chip

Features

- ANSI T1.413 Issue 2 standard DMT modem with embedded, bypassable, ATM framer
- Byte interface or standard Utopia level 1 and level 2 ATM interfaces
- Main functions include:

Receive Direction:

- Rotor and adaptive frequency domain equalizing
- Demapping of DMT carriers into a digital bitstream, including 4D trellis coding
- Error and noise monitoring on individual carriers and pilot tones
- Reed-Solomon decoding and deinterleaving
- ADSL deframing
- ATM cell-specific deframing (can be bypassed)
- 144-pin PQFP package
- Power consumption 1 watt at 3.3V

Transmit Direction:

- ATM cell-specific framing
- ADSL framing
- Reed-Solomon encoding
- Mapping of digital bitstream onto DMT carriers
- Rotor and frequency domain gain correction

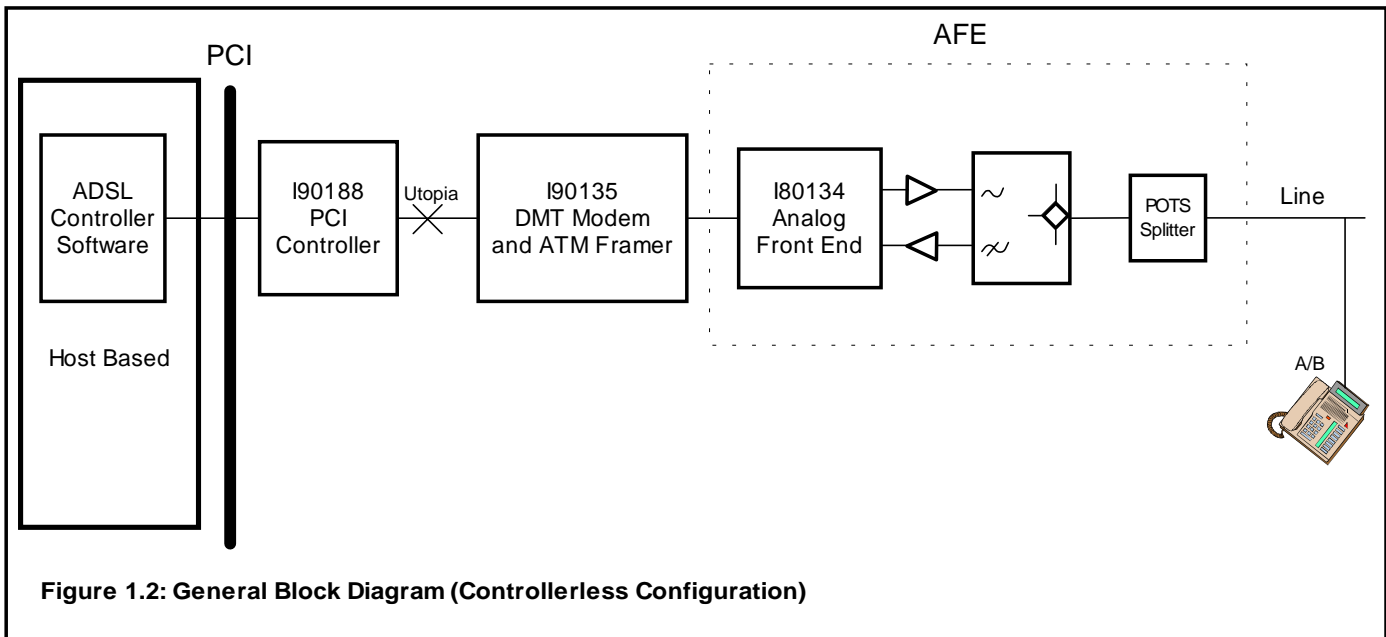
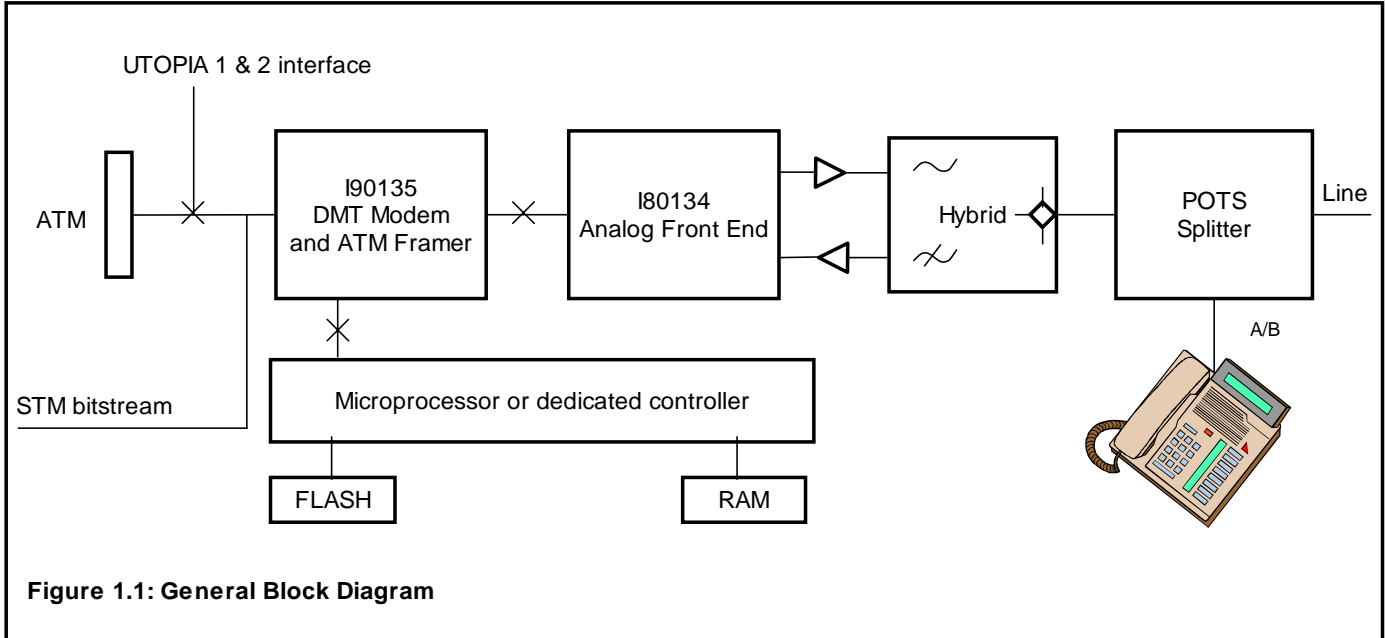
General Description

ITeX's I90135 is the DMT modem and ATM Frammer of the Apollo series rate adaptive ADSL chipset. The I90135 is intended to be used in combination with I80134 analog front end. In addition, the control function of the chipset can be performed on a dedicated external controller (see figure 1.1) or on host/control software eliminating the need for a microcontroller (see figure 1.2).

The I90135 may be used in both ATU-C (central office) and ATU-R (remote) applications. The chip provides both a cell-based UTOPIA level 1 and 2 ATM data interface to the host and a non-ATM synchronous bit stream.

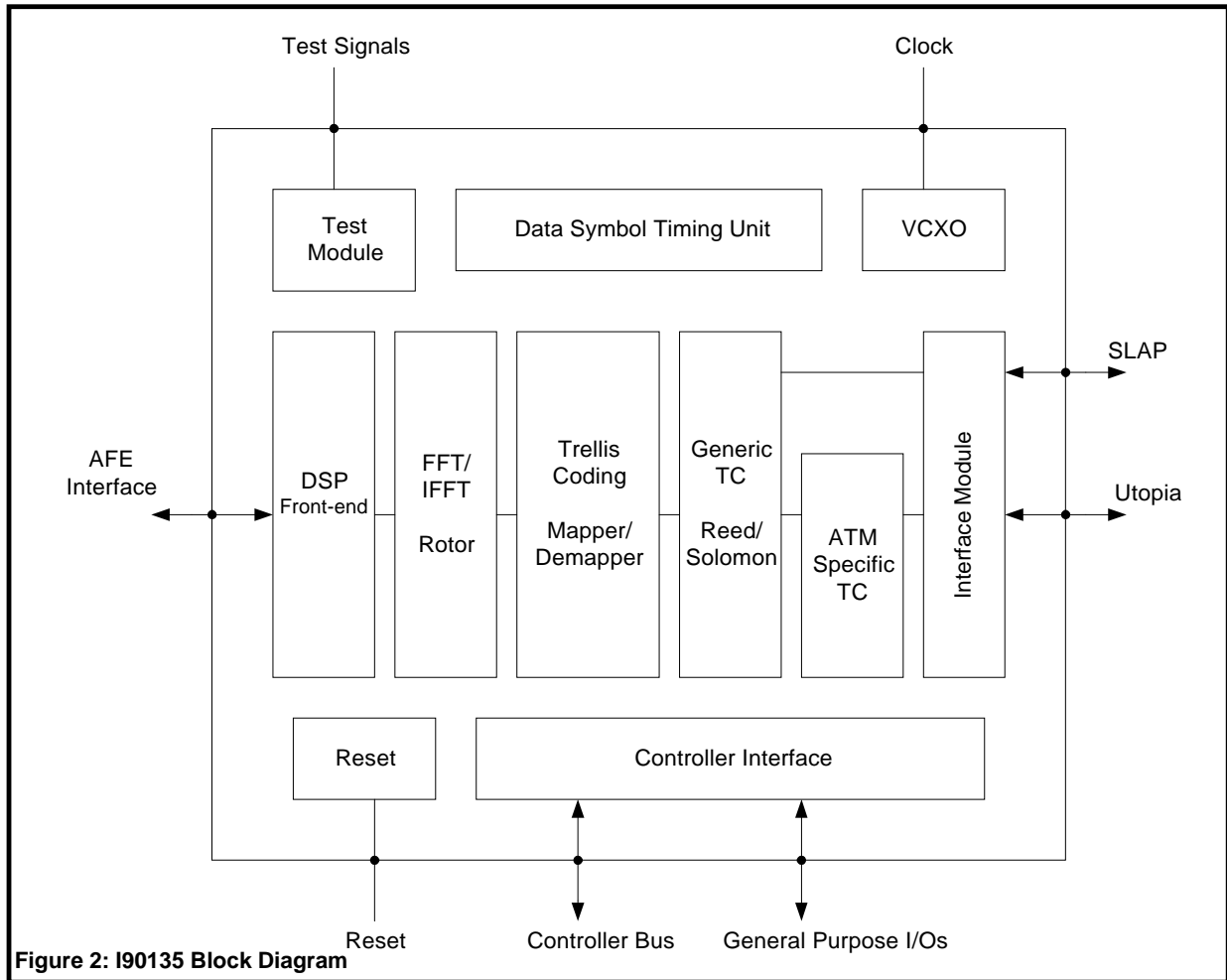
The I90135 performs the DMT modulation, demodulation, Reed-Solomon encoding, bit interleaving, and 4D trellis coding.

The I90135 is in a 144-pin PQFP package.





Block Diagram



Introduction

The following essential describes the sequence of actions for the receive direction, corresponding functions for the transmit direction are readily derived.

DSP Front End

The DSP front end contains four parts in the receive direction: the input selector, the analog front end interface, the decimator and the time equalizer. The input selector

is used internally to enable test loopbacks inside the chip. The analog front end interface transfers 16-bit word, multiplexed on four input/output signals. As a result, four dock cycles are needed to transfer one word. The decimator receives the 16-bit samples at 8.8 MHz (as sent by the analog front end chip) and reduces this rate to 2.2 MHz.



The Time Equalizer (TEQ) module is an FIR filter with programmable coefficients. Its main purpose is to reduce the effect of Inter-Symbol Interferences (ISI) by shortening the channel impulse response. Both the decimator and TEQ can be bypassed.

In the transmit direction, the DSP front end includes: sidelobe filtering, clipping, delay equalization, and interpolation. The sidelobe filtering and delay equalization are implemented by IIR filters, reducing the effect of echo in FDM systems.

Clipping is a statistical process limiting the amplitude of the output signal, optimizing the dynamic range of the AFE. The interpolator receives data at 2.2 MHz and generates samples at a rate of 8.8 MHz.

DMT Modem

This computational module is a programmable DSP unit. Its instruction set enables functions like FFT, IFFT, scaling, rotor, and Frequency Equalization (FEQ). This block implements the core of the DMT algorithm as specified in ANSI T1.413.

In the RX path, the 51 2-point FFT transforms the time domain DMT symbol into a frequency domain representation, which can be further decoded by the subsequent demapping stages. After the first stage time domain equalization and FFT block an essentially ICI (InterCarrier Interferences)-free carrier information stream has been obtained. This stream is still affected by carrier-specific channel distortion resulting in an attenuation of the signal amplitude and a rotation of the signal phase. To compensate for these effects,

the FFT is followed by a Frequency Domain Equalizer (FEQ) and a rotor (phase shifter).

In the TX path, the IFFT transforms the DMT symbol generated in the frequency domain by the mapper into a time domain representation. The IFFT block is preceded by a fine tune gain and a rotor stage, allowing for a compensation of the possible frequency mismatch between the master clock frequency and the transmitter clock frequency (which may be locked to another reference). The FFT module is a slave DSP engine controlled by the transceiver controller. It works off line and communicates with the other blocks via buffers controlled by the DSTU block. The DSP executes a program stored in a RAM area, a very flexible implementation open for future enhancements.

DPLL

The Digital PLL module receives a metric for the phase error of the pilot tone. In general, the clock frequencies at the transmitter and receiver do not match exactly. The phase error is filtered and integrated by a low pass filter, yielding an estimation of the frequency offset. Various processes can use this estimate to deal with

the frequency mismatch. In particular, small accumulated phase error can be compensated in the frequency domain by a rotation of the received code constellation (Rotor). Larger errors are compensated in the time domain by inserting or deleting clock cycles in the sample input sequence.



Mapper/Demapper, Monitor, Trellis Coding, FEQ Update

The demapper converts the constellation points computed by the FFT to a block of bits. This essentially consists in identifying a point in a 2D QAM constellation plane. The demapper supports trellis coded demodulation and provides a Viterbi maximum likelihood estimator. When the trellis is active, the demapper receives an indication for the most likely constellation subset to be used. In the transmit direction, the mapper performs the inverse operation, mapping a block of bits into one

constellation point (in a complex $x+jy$ representation) which is passed to the IFFT block. The Trellis Encoder generates redundant bits to improve the robustness of the transmission, using a 4-Dimensional Trellis Coded Modulation scheme. The Monitor computes error parameters for carriers specified in the Demapper process. Those parameters can be used for updates of adaptive filters coefficient, clock phase adjustments, error detection, etc. A series of values is constantly monitored, such as signal power, pilot phase deviations, symbol erasures generation, loss of frame, etc.

Pin Diagram

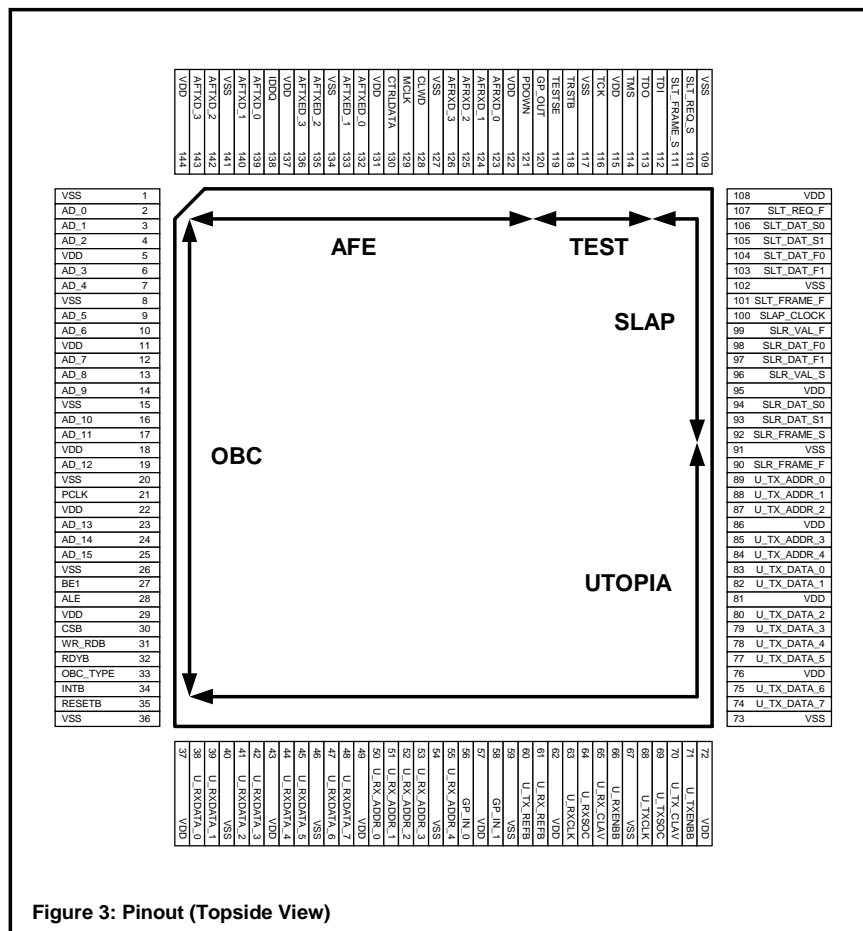


Figure 3: Pinout (Topside View)



Pin Assignment and Description

Pin	Mnemonic	Type	Supply	Driver	BS	Description
1	VSS					0 Volt GROUND
2	AD_0	B	VDD	BD8SCR	B	Micro processor interface
3	AD_1	B	VDD	BD8SCR	B	Address / Data 1
4	AD_2	B	VDD	BD8SCR	B	Address / Data 2
5	VDD					+3.3 Volts power supply
6	AD_3	B	VDD	BD8SCR	B	Address / Data 3
7	AD_4	B	VDD	BD8SCR	B	Address / Data 4
8	VSS					0 Volt GROUND
9	AD_5	B	VDD	BD8SCR	B	
10	AD_6	B	VDD	BD8SCR	B	
11	VDD					+3.3 Volts power supply
12	AD_7	B	VDD	BD8SCR	B	
13	AD_8	B	VDD	BD8SCR	B	
14	AD_9	B	VDD	BD8SCR	B	
15	VSS					0 Volt GROUND
16	AD_10	B	VDD	BD8SCR	B	
17	AD_11	B	VDD	BD8SCR	B	
18	VDD					+3.3 Volts power supply
19	AD_12	B	VDD	BD8SCR	B	
20	VSS					0 Volt GROUND
21	PCLK		VDD	IBUF	I	Processor clock
22	VDD					+3.3 Volts power supply
23	AD_13	B	VDD	BD8SCR	B	
24	AD_14	B	VDD	BD8SCR	B	
25	AD_15	B	VDD	BD8SCR	B	
26	VSS					0 Volt GROUND
27	BE1	I	VDD	IBUF	I	Address [1] input
28	ALE	I	VDD	IBUF	C	Used to latch the address of the internal register to be accessed
29	VDD					+3.3 volts power supply
30	CSB	I	VDD	IBUF	I	Chip selected to respond to bus cycle
31	WR_RDB	I	VDD	IBUF	I	Specifies the direction of the access cycle
32	RDYB	OZ	VDD	BT4CR	O	
33	OBC_TYPE	I-PD	VDD	IBUF	I	ATC Mode Selection
34	INTB	O	VDD	IBUF	O	Requests ATC interrupts service
35	RESETB	I	VDD	IBUF	I	Hard reset
36	VSS					0 Volt GROUND
37	VDD					+3.3 Volts power supply
38	U_RxData_0	OZ	VDD	BD8SCR	B	UTOPIA RX Data 0
39	U_RxData_1	OZ	VDD	BD8SCR	B	UTOPIA RX Data 1



Pin	Mnemonic	Type	Supply	Driver	BS	Description
40	VSS					0 Volt GROUND
41	U_RxData_2	OZ	VDD	BD8SCR	B	UTOPIA RX Data 2
42	U_RxData_3	OZ	VDD	BD8SCR	B	UTOPIA RX Data 3
43	VDD					+3.3 Volts power supply
44	U_RxData_4	OZ	VDD	BD8SCR	B	UTOPIA RX Data 4
45	U_RxData_5	OZ	VDD	BD8SCR	B	UTOPIA RX Data 5
46	VSS					0 Volt GROUND
47	U_RxData_6	OZ	VDD	BD8SCR	B	UTOPIA RX Data 6
48	U_RxData_7	OZ	VDD	BD8SCR	B	UTOPIA RX Data 7
49	VDD					+3.3 Volts power supply
50	U_RxADDR_0	I	VDD	IBUF	I	UTOPIA RX Address 0
51	U_RxADDR_1	I	VDD	IBUF	I	UTOPIA RX Address 1
52	U_RxADDR_2	I	VDD	IBUF	I	UTOPIA RX Address 2
53	U_RxADDR_3	I	VDD	IBUF	I	UTOPIA RX Address 3
54	VSS					0 Volt GROUND
55	U_RxADDR_4	I	VDD	IBUF	I	UTOPIA RX Address 4
56	GP_IN_0	I-PD	VDD	IBUFDQ	I	General purpose input
57	VDD					+3.3 Volts power supply
58	GP_IN_1	I-PD	VDD	IBUFDQ	I	General purpose input 1
59	VSS					0 Volt GROUND
60	U_RxRefB	O	VDD	IBUF	O	8 kHz clock to ATM device
61	U_TxRefB	I	VDD	BT4CR	I	8 kHz from network
62	VDD					VSS +3.3 Volts power supply
63	U_RxCLK	I	VDD	IBUF		Receive interface Utopia clock
64	U_RxSOC	O-Z	VDD	BD8SCR		Receive interface Start of Cell indication
65	U_RxCLAV	O-Z	VDD	BD8SCR		
66	U_RxENBB	I	VDD	IBUF		
67	VSS					0 Volt GROUND
68	U_TxCLK	I	VDD	IBUF		Transmit interface Utopia clock
69	U_TxSOC	I	VDD	IBUF		Transmit interface Start of Cell indication
70	U_TxCLAV	O-Z	VDD	BD8SCR		
71	U_TxENBB	I	VDD	IBUF		UTOPIA TX Enable
72	VDD					+3.3 Volts power supply
73	VSS					0 Volt GROUND
74	U_TxData_7	I	VDD	IBUF	I	UTOPIA TX Data 7
75	U_TxData_6	I	VDD	IBUF	I	UTOPIA TX Data 6
76	VDD					+3.3 Volts power supply
77	U_TxData_5	I	VDD	IBUF	I	UTOPIA TX Data 5
78	U_TxData_4	I	VDD	IBUF	I	UTOPIA TX Data 4
79	U_TxData_3	I	VDD	IBUF	I	UTOPIA TX Data 3
80	U_TxData_2	I	VDD	IBUF	I	UTOPIA TX Data 2
81	VDD					+3.3 Volts power supply



Pin	Mnemonic	Type	Supply	Driver	BS	Description
82	U_TxData_1	I	VDD	IBUF	I	UTOPIA TX Data 1
83	U_TxData_0	I	VDD	IBUF	I	UTOPIA TX Data 0
84	U_TxADDR_4	I	VDD	IBUF	I	UTOPIA TX Address 4
85	U_TxADDR_3	I	VDD	IBUF	I	UTOPIA TX Address 3
86	VDD					+3.3 Volts power supply
87	U_TxADDR_2	I	VDD	IBUF	I	UTOPIA TX Address 2
88	U_TxADDR_1	I	VDD	IBUF	I	UTOPIA TX Address 1
89	U_TxADDR_0	I	VDD	IBUF	I	UTOPIA TX Address 0
90	SLR_FRAME_F	O	VDD	BT4CR		Frame Identifier Fast
91	VSS					0 Volt GROUND
92	SLR_FRAME_S	O	VDD	BT4CR		Frame Identifier Interleaved
93	SLR_DATA_S_1	O	VDD	BT4CR		Data Interleave 1
94	SLR_DATA_S_0	O	VDD	BT4CR		Data Interleave 0
95	VDD					+3.3 Volts power supply
96	SLR_VAL_S	O	VDD	BT4CR		Data Valid Indicator Interleaved
97	SLR_DATA_F_1	O	VDD	BT4CR		Data Fast 1
98	SLR_DATA_F_0	O	VDD	BT4CR		Data Fast 0
99	SLR_VAL_F	O	VDD	BT4CR		Data Valid Indicator Fast
100	SLAP_CLOCK	O	VDD	BT4CR		Clock for SLAP I/F
101	SLT_FRAME_F	O	VDD	BT4CR		Start of Frame Indicator Fast
102	VSS					0 Volt GROUND
103	SLT_DATA_F_1	I	VDD	IBUFDQ		Fast Data 1
104	SLT_DATA_F_0	I	VDD	IBUFDQ		Fast Data 0
105	SLT_DATA_F_1	I	VDD	IBUFDQ		Data 1
106	SLT_DATA_F_0	I	VDD	IBUFDQ		Data 0
107	SLT_REQ_F	O	VDD	BT4CR		Byte Request Fast
108	VDD					+3.3 Volts power supply
109	VSS					0 Volt GROUND
110	SLT_REQ_S	O	VDD	BT4CR		Byte Request Interleaved
111	SLT_FRAME_S	O	VDD	BT4CR		Start of Frame Indication Interleaved
112	TDI	I-PU	VDD	IBUFDQ		JTAG I/P
113	TDO	OZ	VDD	BT4CR		JTAG O/P
114	TMS	I-PU	VDD	IBUFDQ		JTAG Mode Select
115	VDD					+3.3 Volts power supply
116	TCK	I-PD	VDD	IBUFDQ		JTAG Clock
117	VSS					0 Volt GROUND
118	TRSTB	I-PD	VDD	IBUFDQ		JTAG Reset
119	TESTSE	I	VDD	IBUF	none	Enables scan test mode
120	GP_OUT	O	VDD	BD8SCR	O	General purpose analog output
121	PDOWN	O	VDD	BT4CR	O	Power down analog front end
122	VDD					+3.3 Volts power supply
123	AFRXD_0	I	VDD	IBUF	I	Receive data nibble
124	AFRXD_1	I	VDD	IBUF	I	Receive data nibble



Pin	Mnemonic	Type	Supply	Driver	BS	Description
125	AFRXD_2	I	VDD	IBUF	I	Receive data nibble
126	AFRXD_3	I	VDD	IBUF	I	Receive data nibble
127	VSS					0 Volt GROUND
128	CLWD	I	VDD	IBUF	I	Start of word indication
129	MCLK	I	VDD	IBUF	C	Master clock
130	CTRLDATA	O	VDD	BT4CR	O	Serial data transmit channel
131	VDD					+3.3 Volts power supply
132	AFTXD_0	O	VDD	BT4CR	O	Transmit echo nibble
133	AFTXD_1	O	VDD	BT4CR	O	Transmit echo nibble
134	VSS					0 Volt GROUND
135	AFTXD_2	O	VDD	BT4CR	O	Transmit echo nibble
136	AFTXD_3	O	VDD	BT4CR	O	Transmit echo nibble
137	VDD					+3.3 Volts power supply
138	IDDq	I	VDD	IBUF	none	Test pin, active high
139	AFTXD_0	O	VDD	BT4CR	O	Transmit data nibble
140	AFTXD_1	O	VDD	BT4CR	O	Transmit data nibble
141	VSS					0 Volt GROUND
142	AFTXD_2	O	VDD	BT4CR	O	Transmit data nibble
143	AFTXD_3	O	VDD	BT4CR	O	Transmit data nibble
144	VDD					+3.3 Volts power supply

Package

The I90135 is available in a 144-pin PQFP package.

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